

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1. (currently amended) A mixer, comprising:
a track and hold circuit to track and hold a first signal in response to a second signal; and
a bandpass circuit in cooperation with the track and hold circuit,
wherein the track and hold circuit comprises a switch in a path of the first signal, the switch being controlled by the second signal.
2. (original) The mixer of claim 1 further comprising an input circuit to buffer the first signal before being applied to the track and hold circuit.
3. (original) The mixer of claim 1 wherein the track and hold circuit comprises first and second output signals, the mixer further comprising a buffer to combine the first and second output signals.
4. (original) The mixer of claim 1 wherein the bandpass circuit comprises an inductor and capacitor each being coupled to the track and hold circuit, the inductor and capacitor cooperating to provide a time constant related to a frequency of the first signal.
5. (cancelled)
6. (currently amended) The mixer of claim ~~5~~ 1 wherein the switch comprises a transistor having a gate coupled to the second signal.
7. (original) The mixer of claim 6 wherein the transistor further comprises a source coupled

to the first signal.

8. (original) The mixer of claim 7 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

9. (original) The mixer of claim 8 wherein the bandpass circuit further comprises an inductor coupled to the source of the transistor.

10. (original) The mixer of claim 9 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

11. (original) The mixer of claim 7 wherein the bandpass circuit further comprises an inductor coupled to the source of the transistor.

12. (original) The mixer of claim 11 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

13. (original) The mixer of claim 12 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

14. (original) The mixer of claim 1 wherein the track and hold circuit and the bandpass circuit each comprises a differential circuit, the first and second signals each being differential signals.

15. (currently amended) A mixer, comprising:
a track and hold circuit to track and hold a first signal in response to a second signal; and

a bandpass circuit in cooperation with the track and hold circuit,
wherein the track and hold circuit and the bandpass circuit each comprises a differential
circuit, the first and second signals each being differential signals, and

~~The mixer of claim 14~~ wherein the track and hold circuit further comprises a first switch in a first path of a first one of the first differential signals and a second switch in a second path of the first one of the first differential signals, the first switch being controlled by a first one of the second differential signals and the second switch being controlled by a second one of the second differential signals.

16. (original) The mixer of claim 15 wherein the track and hold circuit further comprises a third switch in a first path of a second one of the first differential signals and a fourth switch in a fourth path of the second one of the first differential signals, the third switch being controlled by the first one of the second differential signals and the fourth switch being controlled by a second one of the second differential signals.

17. (original) The mixer of claim 16 wherein the first switch comprises a transistor having a gate coupled to the first one of the second differential signals, the second switch comprises a second transistor having a gate coupled to the second one of the second differential signals, the third switch comprises a third transistor having a gate coupled to the first one of the second differential signals, and the fourth switch comprises a fourth transistor having a gate coupled to the second one of the second differential signals.

18. (original) The mixer of claim 17 wherein the transistors each further comprises a source, the sources of the first and second transistors each being coupled to the first one of the first differential signals and the sources of the third and fourth transistors each being coupled to the second one of the first differential signals.

19. (original) The mixer of claim 18 wherein the bandpass circuit comprises first, second, third and fourth capacitors, wherein the transistors each further comprises a drain, the drain of the first transistor being coupled to the first capacitor, the drain of the second transistor being coupled to the second capacitor, the drain of the third transistor being coupled to the third capacitor, and the drain of the fourth transistor being coupled to the fourth capacitor.

20. (original) The mixer of claim 19 wherein the bandpass circuit further comprises first and second inductors, the first inductor being coupled to the sources of the first and second transistors and the second inductor being coupled to the sources of the third and fourth transistors.

21. (original) The mixer of claim 20 further comprising an input circuit including fifth and sixth transistors each having a drain, the drain of the fifth transistor being coupled to the sources of the first and second transistors and the drain of the sixth transistor being coupled to the sources of the third and fourth transistors.

22. (original) The mixer of claim 18 wherein the first, second, third and fourth transistors each further comprises a drain, the mixer further comprising a buffer to convert voltages at the drains of the first and fourth transistors to a first current and voltages at the drains of the second and third transistors to a second current.

23. (original) The mixer of claim 1 wherein the track and hold circuit comprises a transistor having an input adapted to be coupled to the first signal and an output to generate an output signal in response to the first signal, and a switch in a path of the output signal, the switch being controlled by the second signal.

24. (original) The mixer of claim 23 wherein the switch comprises a second transistor having a gate coupled to the second signal.

25. (original) The mixer of claim 24 wherein the second transistor further comprises a drain coupled to the output of the transistor.

26. (original) The mixer of claim 25 wherein the bandpass circuit comprises a capacitor coupled to the output of the transistor.

27. (original) The mixer of claim 26 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the source of the second transistor.

28. (original) The mixer of claim 27 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

29. (original) The mixer of claim 25 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the source of the second transistor.

30. (original) The mixer of claim 29 wherein the bandpass circuit comprises a capacitor coupled to the output of the transistor.

31. (original) The mixer of claim 30 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

32. (original) The mixer of claim 1 wherein the track and hold circuit and the bandpass circuit each comprises a differential circuit, the first and second signals each being differential signals.

33. (previously presented) A mixer, comprising:
a track and hold circuit to track and hold a first signal in response to a second signal; and
a bandpass circuit in cooperation with the track and hold circuit,
wherein the track and hold circuit and the bandpass circuit each comprises a differential circuit, the first and second signals each being differential signals,

wherein the track and hold circuit comprises a first transistor having a first input adapted to be coupled to a first one of the first differential signals and a first output to generate a first output signal in response to the first one of the first differential signals, a second transistor having a second input adapted to be coupled to the first one of the first differential signals and a second output to generate a second output signal in response to the first one of the first differential signals, a third transistor having a third input adapted to be coupled to a second one of the first differential signals and a third output to generate a third output signal in response to the second one of the first differential signals, and a fourth transistor having a fourth input adapted to be coupled to the second one of the first differential signals and a fourth output to generate a fourth output signal in response to the second one of the first differential signals, wherein the track and the hold circuit further comprises a first switch in a path of the first output signal, a second switch in a path of the second output signal, a third switch in a path of the third output signal, and a fourth switch in a path of the fourth output signal, the first switch being controlled by a first one of the second differential signals, the second switch being controlled by a second one of the second differential signals, the third switch being controlled by the first one of the second differential signals, and the fourth switch being controlled by the second one of the second differential signals.

34. (original) The mixer of claim 33 wherein the first switch comprises a fifth transistor having a gate coupled to the first one of the second differential signals, the second switch comprises a sixth transistor having a gate coupled to the second one of the second differential signals, the third switch comprises a seventh transistor having a gate coupled to the first one of the second differential signals, and the fourth switch comprises an eighth transistor having a gate coupled to the second one of the second differential signals.

35. (original) The mixer of claim 34 wherein the bandpass circuit further comprises a first capacitor coupled to the first output of the first transistor, a second capacitor coupled to the second output of the second transistor, a third capacitor coupled to the third output of the third transistor, and a fourth capacitor coupled to the fourth output of the fourth transistor.

36. (original) The mixer of claim 35 wherein the fifth, sixth, seventh and eighth transistors each comprises a drain and source, the drain of the fifth transistor being coupled to the first capacitor, the drain of the sixth capacitor being coupled to the second capacitor, the drain of the seventh transistor being coupled to the third capacitor, and the drain of the eighth transistor being coupled to the fourth transistor, the bandpass circuit further comprising a first inductor coupled to the drain of the fifth transistor, the bandpass circuit further comprising a first inductor coupled to the drain of the fifth transistor, a second inductor coupled to the drain of the sixth transistor, a third inductor coupled to the drain of the seventh transistor, and a fourth inductor coupled to the drain of the eighth transistor.

37. (original) The mixer of claim 36 wherein each of the first, second, third and fourth transistors comprises a source, the source of the first and third transistors being coupled together and the sources of the second and fourth transistors being coupled together, the mixer further comprising a fifth switch coupled to the common sources of the first and third transistors, and a sixth switch

coupled to the common sources of the second and fourth transistors, the fifth switch being controlled by the first one of the second differential signals and the sixth switch being controlled by the second one of the second differential signals.

38. (original) The mixer of claim 37 further comprising a buffer to convert voltages at the first and fourth outputs to a first current and voltages at the second and third outputs to a second current.

39. (currently amended) A mixer, comprising:
a track and hold circuit having a signal input, a control input, and a mixed signal output; and
a bandpass circuit coupled to the signal input and the mixed signal output,
wherein the track and hold circuit comprises a switch between the signal input and the mixed signal output, the switch being controlled by the control input.

40. (original) The mixer of claim 39 further comprising an input circuit coupled to the signal input.

41. (original) The mixer of claim 39 wherein the mixed signal output comprises first and second output signals, the mixer further comprising a buffer to combine the first and second output signals.

42. (original) The mixer of claim 39 wherein the bandpass circuit comprises an inductor coupled to the signal input and a capacitor coupled to the mixed signal output.

43. (cancelled)

44. (currently amended) The mixer of claim ~~43~~ 39 wherein the switch comprises a transistor having a gate coupled to the control input.

45. (original) The mixer of claim 44 wherein the transistor further comprises a source coupled to the signal input.

46. (original) The mixer of claim 45 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

47. (original) The mixer of claim 46 wherein the bandpass circuit further comprises an inductor coupled to the signal input.

48. (original) The mixer of claim 47 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

49. (original) The mixer of claim 45 wherein the bandpass circuit further comprises an inductor coupled to the signal input.

50. (original) The mixer of claim 49 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

51. (original) The mixer of claim 50 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

52. (original) The mixer of claim 39 wherein the track and hold circuit comprises a transistor having an input coupled to the signal input and an output coupled to the mixed signal output, and a

current source coupled to the mixed signal output, the current source being controlled by the control input.

53. (currently amended) A mixer, comprising:

a track and hold circuit having a signal input, a control input, and a mixed signal output; and

a bandpass circuit coupled to the signal input and the mixed signal output,

wherein the track and hold circuit comprises a transistor having an input coupled to the signal input and an output coupled to the mixed signal output, and a current source coupled to the mixed signal output, the current source being controlled by the control input, and

~~The mixer of claim 52~~ wherein the current source comprises a second transistor having a gate coupled to the control input.

54. (original) The mixer of claim 53 wherein the second transistor further comprises a drain coupled to the mixed signal output.

55. (original) The mixer of claim 54 wherein the bandpass circuit comprises a capacitor coupled to the mixed signal output.

56. (original) The mixer of claim 55 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the drain of the second transistor.

57. (original) The mixer of claim 56 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

58. (original) The mixer of claim 55 wherein the second transistor further comprises a

source, and the bandpass circuit further comprises an inductor coupled to the source of the second transistor.

59. (original) The mixer of claim 58 wherein the bandpass circuit comprises a capacitor coupled to the mixed signal output.

60. (original) The mixer of claim 59 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

61. (cancelled).

62. (currently amended) A differential mixer, comprising:
a track and hold circuit having a differential signal input, a differential control input, and a
differential mixed signal output; and
a bandpass circuit coupled to the differential signal input and the differential mixed signal
output.

~~The mixer of claim 61~~ wherein the track and hold circuit further comprises a first switch between a first one of the differential inputs and a first one of the differential mixed signal outputs, and a second switch between the first one of the differential inputs and the first one of the differential mixed signal outputs, the first switch being controlled by a first one of the differential control inputs and the second switch being controlled by a second one of the differential control inputs.

63. (original) The mixer of claim 62 wherein the track and hold circuit further comprises a third switch between a second one of the differential inputs and a second one of the differential mixed signal outputs, and a fourth switch between the second one of the differential inputs and the

second one of the differential mixed signal outputs, the third switch being controlled by a first one of the differential control inputs and the fourth switch being controlled by a second one of the differential control inputs.

64. (original) The mixer of claim 63 wherein the first switch comprises a transistor having a gate coupled to the first one of the differential control inputs, the second switch comprises a second transistor having a gate coupled to the second one of the differential control inputs, the third switch comprises a third transistor having a gate coupled to the first one of the differential control inputs, and the fourth switch comprises a fourth transistor having a gate coupled to the second one of the differential control inputs.

65. (original) The mixer of claim 64 wherein the transistors each further comprises a source, the sources of the first and second transistors each being coupled to the first one of the differential signal inputs and the sources of the third and fourth transistors each being coupled to the second one of the differential signal inputs.

66. (original) The mixer of claim 65 wherein the bandpass circuit comprises first, second, third and fourth capacitors, wherein the transistors each further comprises a drain, the drain of the first transistor being coupled to the first capacitor, the drain of the second transistor being coupled to the second capacitor, the drain of the third transistor being coupled to the third capacitor, and the drain of the fourth transistor being coupled to the fourth capacitor.

67. (original) The mixer of claim 66 wherein the bandpass circuit further comprises first and second inductors, the first inductor being coupled to the sources of the first and second transistors and the second inductor being coupled to the sources of the third and fourth transistors.

68. (original) The mixer of claim 67 further comprising an input circuit including fifth and sixth transistors each having a drain, the drain of the fifth transistor being coupled to the sources of the first and second transistors and the drain of the sixth transistor being coupled to the sources of the third and fourth transistors.

69. (original) The mixer of claim 68 wherein the first, second, third and fourth transistors each further comprises a drain, the mixer further comprising a buffer to convert voltages at the drains of the first and fourth transistors to a first current and voltages at the drains of the second and third transistors to a second current.

70. (previously presented) A differential mixer, comprising:

a track and hold circuit having a differential signal input, a differential control input, and a differential mixed signal output; and

a bandpass circuit coupled to the differential signal input and the differential mixed signal output,

wherein the track and hold circuit comprises a first transistor having a first input coupled to a first one of the differential signal inputs and a first output, a second transistor having a second input coupled to the first one of the differential signal inputs and a second output, a third transistor having a third input coupled to a second one of the differential signal inputs, and a fourth transistor having a fourth input coupled to the second one of the differential signal inputs, wherein the track and hold circuit further comprises a first switch coupled to the first output, a second switch coupled to the second output, a third switch coupled to the third output, and a fourth switch coupled to the fourth output the first switch being controlled by a first one of the differential control inputs, the second switch being controlled by a second one of the differential control inputs, the third switch being controlled by the first one of the differential control inputs, and the fourth switch being controlled by the second one of the differential control inputs.

71. (original) The mixer of claim 70 wherein the first switch comprises a fifth transistor having a gate coupled to the first one of the differential control inputs, the second switch comprises a sixth transistor having a gate coupled to the second one of the differential control inputs, the third switch comprises a seventh transistor having a gate coupled to the first one of the differential control inputs, and the fourth switch comprises an eighth transistor having a gate coupled to the second one of the differential control inputs.

72. (original) The mixer of claim 71 wherein the bandpass circuit further comprising a first capacitor coupled to the first output of the first transistor, a second capacitor coupled to the second output of the second transistor, a third capacitor coupled to the third output of the third transistor, and a fourth capacitor coupled to the fourth output of the fourth transistor.

73. (original) The mixer of claim 72 wherein the fifth, sixth, seventh, and eighth transistors each comprises a drain and source, the drain of the fifth transistor being coupled to the first capacitor, the drain of the sixth transistor being coupled to the second capacitor, the drain of the seventh transistor being coupled to the third capacitor, and the drain of the eighth transistor being coupled to the fourth capacitor, the bandpass circuit further comprising a first inductor coupled to the drain of the fifth transistor, a second inductor coupled to the drain of the sixth transistor, a third inductor coupled to the drain of the seventh transistor, and a fourth inductor coupled to the drain of the eighth transistor.

74. (original) The mixer of claim 73 wherein each of the first, second, third and fourth transistors comprises a source, the source of the first and third transistors being coupled together and the sources of the second and fourth transistors being coupled together, the mixer further comprising a fifth switch coupled to the common sources of the first and third transistors, and a sixth switch

coupled to the common sources of the second and fourth transistors, the fifth switch being controlled by the first one of the differential control inputs and the sixth switch being controlled by the second one of the differential control input.

75. (original) The mixer of claim 74 further comprising a buffer to convert voltages at the first and fourth outputs to a first current and voltages at the second and third outputs to a second current.

Claims 76-93 (cancelled)

94. (new) The mixer of claim 1 wherein the mixer is part of a phase locked loop.

95. (new) The mixer of claim 1 wherein the mixer is part of a phase locked loop that employs complementary metal oxide semiconductor (CMOS) technology.

96. (new) The mixer of claim 1 wherein the mixer is part of a transmitter in a wireless communications device.

97. (new) The mixer of claim 1 wherein the mixer is part of a single integrated circuit chip transceiver in a wireless communications device.

98. (new) The mixer of claim 1 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless spread spectrum communications.

99. (new) The mixer of claim 1 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless direct sequence spread spectrum communications.

100. (new) The mixer of claim 1 wherein the mixer is part of a transceiver in a wireless communications device that supports frequency hopping.

101. (new) The mixer of claim 1 wherein the mixer is part of a transceiver in a wireless communications device that employs complementary metal oxide semiconductor (CMOS) technology.

102. (new) The mixer of claim 101 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless local area network communications.

103. (new) The mixer of claim 101 wherein the mixer is part of a transceiver in a wireless communications device that supports Bluetooth communications.

104. (new) The mixer of claim 101 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless 802.11 communications.

105. (new) The mixer of claim 101 wherein the mixer is part of a transceiver in a wireless communications device that supports orthogonal frequency division modulation.

106. (new) The mixer of claim 39 wherein the mixer is part of a phase locked loop.

107. (new) The mixer of claim 39 wherein the mixer is part of a complementary metal oxide semiconductor (CMOS) phase locked loop.

108. (new) The mixer of claim 39 wherein the mixer is part of a transmitter in a wireless

communications device.

109. (new) The mixer of claim 39 wherein the mixer is part of a single integrated circuit chip transceiver in a wireless communications device.

110. (new) The mixer of claim 39 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless spread spectrum communications.

111. (new) The mixer of claim 39 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless direct sequence spread spectrum communications.

112. (new) The mixer of claim 39 wherein the mixer is part of a transceiver in a wireless communications device that supports frequency hopping.

113. (new) The mixer of claim 39 wherein the mixer is part of a transceiver in a wireless communications device that employs complementary metal oxide semiconductor (CMOS) technology.

114. (new) The mixer of claim 113 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless local area network communications.

115. (new) The mixer of claim 113 wherein the mixer is part of a transceiver in a wireless communications device that supports Bluetooth communications.

116. (new) The mixer of claim 113 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless 802.11 communications.

117. (new) The mixer of claim 113 wherein the mixer is part of a transceiver in a wireless communications device that supports orthogonal frequency division modulation.

118. (new) The mixer of claim 53 wherein the mixer is part of a phase locked loop.

119. (new) The mixer of claim 53 wherein the mixer is part of a phase locked loop that employs complementary metal oxide semiconductor (CMOS) technology.

120. (new) The mixer of claim 53 wherein the mixer is part of a transmitter in a wireless communications device.

121. (new) The mixer of claim 53 wherein the mixer is part of a single integrated circuit chip transceiver in a wireless communications device.

122. (new) The mixer of claim 53 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless spread spectrum communications.

123. (new) The mixer of claim 53 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless direct sequence spread spectrum communications.

124. (new) The mixer of claim 53 wherein the mixer is part of a transceiver in a wireless communications device that supports frequency hopping.

125. (new) The mixer of claim 53 wherein the mixer is part of a transceiver in a wireless communications device that employs complementary metal oxide semiconductor (CMOS)

technology.

126. (new) The mixer of claim 125 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless local area network communications.

127. (new) The mixer of claim 125 wherein the mixer is part of a transceiver in a wireless communications device that supports Bluetooth communications.

128. (new) The mixer of claim 125 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless 802.11 communications.

129. (new) The mixer of claim 125 wherein the mixer is part of a transceiver in a wireless communications device that supports orthogonal frequency division modulation.

130. (new) The mixer of claim 62 wherein the mixer is part of a phase locked loop.

131. (new) The mixer of claim 62 wherein the mixer is part of a phase locked loop that employs complementary metal oxide semiconductor (CMOS) technology.

132. (new) The mixer of claim 62 wherein the mixer is part of a transmitter in a wireless communications device.

133. (new) The mixer of claim 62 wherein the mixer is part of a single integrated circuit chip transceiver in a wireless communications device.

134. (new) The mixer of claim 62 wherein the mixer is part of a transceiver in a wireless

communications device that supports wireless spread spectrum communications.

135. (new) The mixer of claim 62 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless direct sequence spread spectrum communications.

136. (new) The mixer of claim 62 wherein the mixer is part of a transceiver in a wireless communications device that supports frequency hopping.

137. (new) The mixer of claim 62 wherein the mixer is part of a transceiver in a wireless communications device that employs complementary metal oxide semiconductor (CMOS) technology.

138. (new) The mixer of claim 137 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless local area network communications.

139. (new) The mixer of claim 137 wherein the mixer is part of a transceiver in a wireless communications device that supports Bluetooth communications.

140. (new) The mixer of claim 137 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless 802.11 communications.

141. (new) The mixer of claim 137 wherein the mixer is part of a transceiver in a wireless communications device that supports orthogonal frequency division modulation.

142. (new) The mixer of claim 15 wherein the mixer is part of a phase locked loop.

143. (new) The mixer of claim 15 wherein the mixer is part of a phase locked loop that employs complementary metal oxide semiconductor (CMOS) technology.

144. (new) The mixer of claim 15 wherein the mixer is part of a transmitter in a wireless communications device.

145. (new) The mixer of claim 15 wherein the mixer is part of a single integrated circuit chip transceiver in a wireless communications device.

146. (new) The mixer of claim 15 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless spread spectrum communications.

147. (new) The mixer of claim 15 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless direct sequence spread spectrum communications.

148. (new) The mixer of claim 15 wherein the mixer is part of a transceiver in a wireless communications device that supports frequency hopping.

149. (new) The mixer of claim 15 wherein the mixer is part of a transceiver in a wireless communications device that employs complementary metal oxide semiconductor (CMOS) technology.

150. (new) The mixer of claim 149 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless local area network communications.

151. (new) The mixer of claim 149 wherein the mixer is part of a transceiver in a wireless

communications device that supports Bluetooth communications.

152. (new) The mixer of claim 149 wherein the mixer is part of a transceiver in a wireless communications device that supports wireless 802.11 communications.

153. (new) The mixer of claim 149 wherein the mixer is part of a transceiver in a wireless communications device that supports orthogonal frequency division modulation.

154. (new) A wireless communications device that supports wireless spread spectrum communications, comprising:

a phase locked loop that comprises

a mixing circuit arrangement that comprises

a track and hold circuit to track and hold a first signal in response to a second signal, and

a bandpass circuit in cooperation with the track and hold circuit,

wherein the track and hold circuit comprises a switch in a path of the first signal, the switch being controlled by the second signal.

155. (new) The wireless communications device of claim 154, wherein the phase locked loop is part of a single integrated circuit chip transceiver that employs complementary metal oxide semiconductor (CMOS) technology.

156. (new) The wireless communications device of claim 155, wherein the wireless communications device supports one or more of the following: Bluetooth communications, wireless 802.11 communications, wireless local area network communications and wireless personal area network communications.

157. (new) The wireless communications device of claim 154, wherein the wireless spread spectrum communications employs one or more of the following: direct sequence spread spectrum communications and frequency hopping communications.

158. (new) The wireless communications device of claim 154,
wherein phase locked loop employs complementary metal oxide semiconductor (CMOS) technology, and
wherein the wireless communications device supports Bluetooth communications.

159. (new) A wireless communications device that supports wireless spread spectrum communications, comprising:
a wireless transceiver that comprises
 a mixing circuit arrangement that comprises
 a track and hold circuit having a signal input, a control input, and a mixed signal output, and
 a bandpass circuit coupled to the signal input and the mixed signal output,
wherein the track and hold circuit comprises a switch between the signal input and the mixed signal output, the switch being controlled by the control input.

160. (new) The wireless communications device of claim 159, wherein the wireless transceiver is a single integrated circuit chip transceiver that employs complementary metal oxide semiconductor (CMOS) technology.

161. (new) The wireless communications device of claim 160, wherein the wireless communications device supports one or more of the following: Bluetooth communications, wireless

802.11 communications, wireless local area network communications and wireless personal area network communications.

162. (new) The wireless communications device of claim 159,
wherein the wireless spread spectrum communications employs one or more of the following: direct sequence spread spectrum communications and frequency hopping communications, and
wherein the wireless communications device employs complementary metal oxide semiconductor (CMOS) technology.

163. (new) The wireless communications device of claim 159,
wherein the wireless communications device employs complementary metal oxide semiconductor (CMOS) technology, and
wherein the wireless communications device supports Bluetooth communications.